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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,307	12/23/2003	Qi Zhang	P-6215-US	5556

49444   7590   01/25/2007

PEARL COHEN ZEDEK LATZER, LLP
1500 BROADWAY, 12TH FLOOR
NEW YORK, NY 10036

EXAMINER
CHAVIS, JOHN Q

ART UNIT	PAPER NUMBER
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	10/743,307	ZHANG ET AL.
	Examiner	Art Unit	
	John Chavis	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _23 December 2003_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-26_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-26_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _23 December 2003_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _6/27/06_.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dhablania (6,965,906) in view of the non patent literature reference cited by the

applicant as 43258.

1. A <u>What is claimed is:</u>	<u>Dhablania/43258</u>
method comprising: translating	See the title and the abstract.
a first sequence of instructions	
associated with a source architecture	
into a second sequence of instructions	
associated with a target architecture,	
wherein said first sequence includes	See page 1 line 65-page 2 line 11,
one or more floating point control	decimal instructions are considered
instructions and said second sequence	not to include a floating point
does not include a floating point	control instruction.
control instruction, and	
wherein results produced by	See the summary of the invention.

executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.

Assuming that the applicant does not believe that Dhablania's system provides for " substantially the same results, the feature is considered to be provided by the non patent literature " Rounding mode independent implementation of float to integer truncation (43258). Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to utilize the feature in Dhablania's system for the same reason to acquire substantially the same results by enabling selection of the desired mode of rounding to provide the desired results.

2. The method of claim 1, wherein said second sequence includes an instruction to round an initial floating point number to a first floating point number using round to zero rounding mode, regardless of a rounding mode

See the 43258 reference.

setting of the target architecture.

Some mode has to be selected and each mode provides substantially similar results. Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to select a specific rounding mode for use in Dhablania's system to provide a certain precision desired, see again the 43258 reference.

3. The method of claim 1, wherein said first sequence of instructions and said second sequence of instructions are binary code.

Code submitted to a computer is considered binary code and therefore this feature is considered inherent to Both cited references (for example, see as an example only the Hanson reference (5,652,862; col. 1 lines 19-22.

4. The method of claim 1, further comprising: identifying in said first sequence a rounding mode of one of said one or more floating point control instructions.

See the first page of the 43258 reference, specifically the third para.

In reference to claims 5-8, 9-14, 15-17, 18-20, 21-23 and 24-26, see the rejections of claim 1-4 above and again note that reference 43258 provides for selection of modes (which is merely considered a choice of design; since, some mode has to be

utilized and the mode selected is considered to be based on the level of precision

desired.

3.   Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Abdullah et al. (6,502,115) and further in view of 43258.

1. A <u>What is claimed is</u>:	Abdullah/43258
method comprising: translating	See the title and the abstract.
a first sequence of instructions	
associated with a source architecture	
into a second sequence of instructions	
associated with a target architecture,	
wherein said first sequence includes	See figs. 11 & 13, Abdullah' s integer
one or more floating point control	instructions are considered
instructions and said second sequence	not to include a floating point
does not include a floating point	control instruction.
control instruction, and	
wherein results produced by	See the summary of the invention.
executing said second sequence on a	Assuming that the applicant does not
processor that complies with said	believe that Abdullah' s system
target architecture are substantially the	provides for " substantially the same
same as results produced by executing	results, the feature is considered to

said first sequence on a processor that

complies with said source architecture.

be provided by the non patent literature

" Rounding mode independent

implementation of float to integer

truncation (43258). Therefore, it would

have been obvious to a person having

ordinary skill in the art at the time of the

invention to utilize the feature in

Abdullah' s system for the same

reason to acquire substantially the same

results by enabling selection of the

desired mode of rounding to provide the

desired results.

2. The method of claim 1, wherein

said second sequence includes an

instruction to round an initial floating

point number to a first floating point

number using round to zero rounding

mode, regardless of a rounding mode

setting of the target architecture.

See the 43258 reference.

Some mode has to be selected and

each mode provides substantially similar

results. Therefore, it would have been

obvious to a person having ordinary skill

in the art at the time of the invention to

select a specific rounding mode for use

in Abdullah' s system to provide a

	certain precision desired, see again the 43258 reference.
3. The method of claim 1, wherein said first sequence of instructions and said second sequence of instructions are binary code.	Code submitted to a computer is considered binary code and therefore this feature is considered inherent to Both cited references (for example, see as an example only the Hanson reference (5,652,862; col. 1 lines 19-22.
4. The method of claim 1, further comprising: identifying in said first sequence a rounding mode of one of said one or more floating point control instructions.	See the first page of the 43258 reference, specifically the third para.

In reference to claims 5-8, 9-14, 15-17, 18-20, 21-23 and 24-26, see the rejections of claim 1-4 above and again note that reference 43258 provides for selection of modes (which is merely considered a choice of design; since, some mode has to be utilized and the mode selected is considered to be based on the level of precision desired.

4.   Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman (6,131,104) and further in view of 43258.

1. A What is claimed is:	Oberman/43258

method comprising: translating a first sequence of instructions associated with a source architecture into a second sequence of instructions associated with a target architecture,	See the title and the abstract.
wherein said first sequence includes one or more floating point control instructions and said second sequence does not include a floating point control instruction, and	See the background of the invention.
wherein results produced by executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.	See the summary of the invention. Assuming that the applicant does not believe that Oberman' s system provides for " substantially the same results, the feature is considered to be provided by the non patent literature " Rounding mode independent implementation of float to integer truncation (43258). Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the

invention to utilize the feature in Oberman' s system for the same reason to acquire substantially the same results by enabling selection of the desired mode of rounding to provide the desired results.

2. The method of claim 1, wherein said second sequence includes an instruction to round an initial floating point number to a first floating point number using round to zero rounding mode, regardless of a rounding mode setting of the target architecture.

See the 43258 reference.

Some mode has to be selected and each mode provides substantially similar results. Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to select a specific rounding mode for use in Oberman' s system to provide a certain precision desired, see again the 43258 reference.

3. The method of claim 1, wherein said first sequence of instructions and said second sequence of instructions

Code submitted to a computer is considered binary code and therefore this feature is considered inherent to

are binary code.

Both cited references (for example, see

as an example only the Hanson

reference (5,652,862; col. 1 lines 19-22.

4. The method of claim 1, further

See the first page of the 43258

comprising: identifying in said first

reference, specifically the third para.

sequence a rounding mode of one of

said one or more floating point

control instructions.

In reference to claims 5-8, 9-14, 15-17, 18-20, 21-23 and 24-26, see the

rejections of claim 1-4 above and again note that reference 43258 provides for selection

of modes (which is merely considered a choice of design; since, some mode has to be

utilized and the mode selected is considered to be based on the level of precision

desired.

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to John Chavis whose telephone number is (571) 272-

3720. The examiner can normally be reached on M-F, 9:00am-5:30pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JC

John Chavis
Primary Examiner AU-2193